Notice of Allowability	Application No.	Applicant(s)	
	10/629,596	SHIOZAWA ET AL.	
	Examiner	Art Unit	
	Julia P. Tu	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *03/23/2007*.

2. ☒ The allowed claim(s) is/are *1-6*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Carl J. Pellegrini on April 25, 2007.

In claim 1, change "transmitting said time information RTSs" on line 4 to "transmitting said parallel data and said time information RTSs".

In claims 2 and 3, change "Mq – 2 (p-1)" in claim 2 on lines 6-7 of page 5 and in claim 3, line 3 to "Mq- $2^{(p-1)}$".

2. The following is an examiner's statement of reasons for allowance:

(1) regarding claim 1:

The present invention comprises a serial digital signal transmission system comprising a residual time stamp (RTS) generator circuit for separating high definition television (HDTV) serial digital signals to be transmitted into parallel data and time information residual time stamps (RTSs) and transmitting them as separated, and an RTS receiver circuit for receiving said parallel data and said time information RTSs that have been transmitted and obtaining said HDTV serial digital signals as they were originally, wherein: said RTS generator circuit has: first frequency dividing means for dividing a network clock into a prescribed first frequency, a serial-to-parallel converter

for subjecting said HDTV serial digital signals to be transmitted to serial-to-parallel conversion, transmitting data of the resultant parallel signals and supplying a clock divided into a second frequency, a first counter for dividing said frequency-divided clock supplied from said serial-to-parallel converter into a 1/N frequency, and a latch circuit for latching at the output timing of said first counter the clock resulting from the frequency division by said first frequency dividing means to supply said time information RTSs, and said RTS receiver circuit comprises: second frequency dividing means for dividing the frequency of said network clock into said prescribed first frequency, gate pulse generating means for generating a gate pulse on the basis of said network clock, memory means for temporarily storing said RTSs which have been transmitted, a comparator for comparing the clock resulting from frequency division by said second frequency dividing means and said RTSs read out of said memory means, a gate circuit for gating the output signal of said comparator on the basis of said gate pulse from said gate pulse generating means, frequency multiplying means for regenerating the clock of said second frequency by multiplying the frequency of the output signal of said gate circuit to said N-multiplied frequency, and a parallel-to-serial converter for receiving as its inputs regenerated clock of said second frequency supplied from said frequency multiplying means and data of said parallel signals that have been transmitted, and subjecting these to parallel-to-serial conversion to obtain said HDTV serial digital signals, 8, 15 or 16 being selected as the value of said N. The closest prior art, Kitagawa et al. and Lau et al disclose a similar system which include frequency dividing circuits, bit counters, and gate pulse generating means but fail to teach N is 8, 15, or 16.

(2) regarding claims 2 and 3:

The present invention comprises first frequency dividing means comprises a first frequency dividing circuit for dividing the network clock into a frequency of 1/32 and a first p-bit counter for counting clocks supplied from the first frequency dividing circuit and obtaining a signal of prescribed first frequency, the second frequency dividing means comprises a second frequency dividing circuit for dividing the network clock into a frequency of 1/32 and a second p-bit counter for counting clocks supplied from the second frequency dividing circuit and obtaining a signal of the prescribed first frequency, the gate pulse generating means is an M.sub.q-2 .sup.(p-1) counter (where M.sub.q is the largest integer that does not surpass the average count M of the clock resulting from frequency division by 32 of the network clock in N periods of the serial clock of HDTV serial digital signals) for counting the clock supplied from said second frequency dividing circuit and supplying said gate pulse, and the frequency multiplying means is a PLL circuit for multiplying the frequency of the output signal of said gate circuit to said N-multiplied frequency. The closest prior art, Kitagawa et al. and Lau et al disclose a similar system which include frequency dividing circuits, bit counters, and gate pulse generating means but fail to teach the dividing circuits which divide the network clock into a frequency of 1/32 and gate pulse generating means is an M.sub.q-2 .sup.(p-1) counter (where M.sub.q is the largest integer that does not surpass the average count M of the clock resulting from frequency division by 32 of the network clock in N periods of the serial clock of HDTV serial digital signals).

(3) regarding claim 4:

Kitagawa et al. and Lau et al further disclose ATM cell processing unit but fail to teach besides selecting 8 as the value of said N, multiplexes 180 bytes of said HDTV serial digital signals on four of said ATM cells to generate ATM cells on whose remainder of payload are multiplexed nine of said time information RTSs corresponding to the 180 bytes of HDTV serial digital signals. The distinct features have been added to the independent claim 4, therefore, rendering them allowable.

(4) regarding claim 5:

Kitagawa et al. and Lau et al. also fail to teach the ATM cell processing unit, besides selecting 8 as the value of N, multiplexes 5500 bytes of said HDTV serial digital signals on 123 of ATM cells to generate ATM cells on whose remainder of payload are multiplexed 275 of time information RTSs corresponding to the 5500 bytes of HDTV serial digital signals. The distinct features have been added to the independent claim 5, therefore, rendering them allowable.

(5) regarding claim 6:

Kitagawa et al. and Lau et al. also fail to teach said ATM cell processing unit, besides selecting 15 as the value of N, multiplexes 375 bytes of HDTV serial digital signals on eight of ATM cells to generate ATM cells on whose remainder of payload and RTS area of Segmentation and Reassembly Protocol Data Unit (SAR-PDU) header are multiplexed 10 of said time information RTSs corresponding to the 375 bytes of HDTV serial digital signals. The distinct features have been added to the independent claim 6, therefore, rendering them allowable.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Julia P. Tu whose telephone number is 571-270-1087. The examiner can normally be reached on 7:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

J.T.

04/17/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER